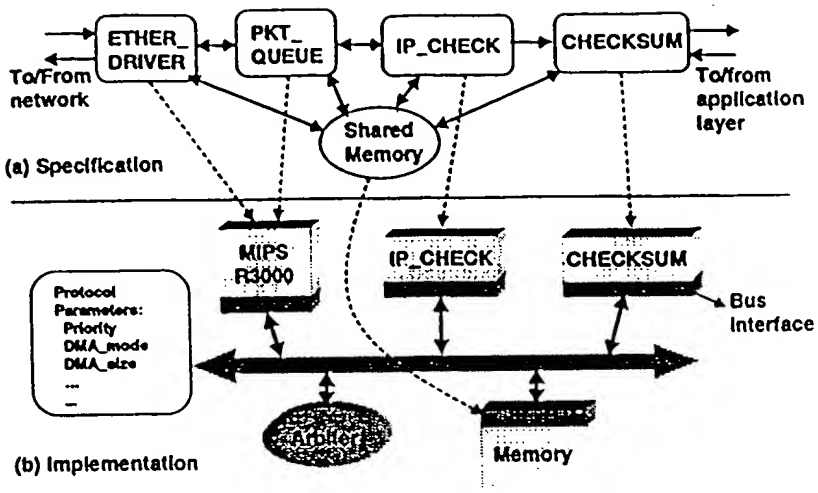

ETHER_ DRIVER
PKT_ QUEUE
IP_CHECK
CHECKSUM
To/From network
To/from application layer
Shared Memory
(a) Specification
MIPS R3000
IP_CHECK
CHECKSUM
Bus Interface
Protocol Parameters:
Priority
DMA_mode
DMA_size
...
Arbiter
Memory
(b) Implementation

FIG. 1

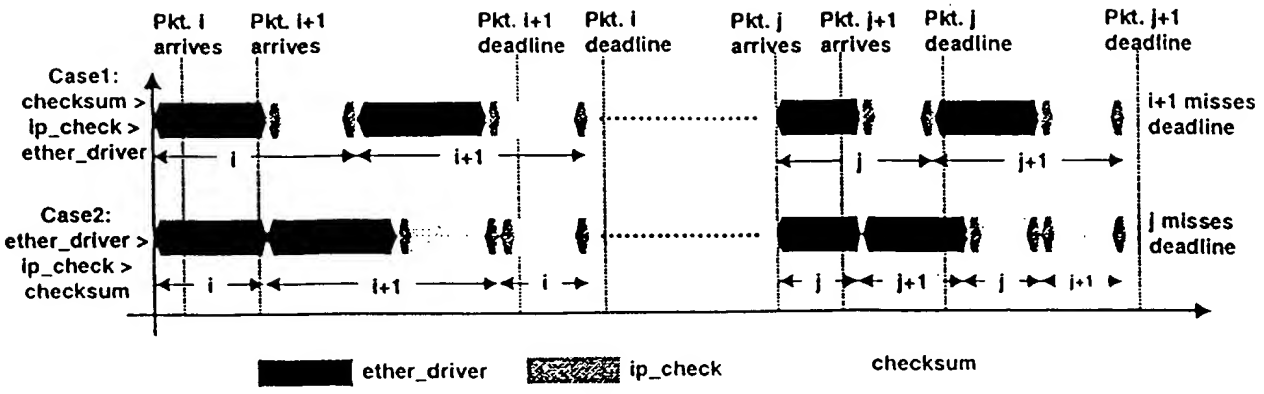
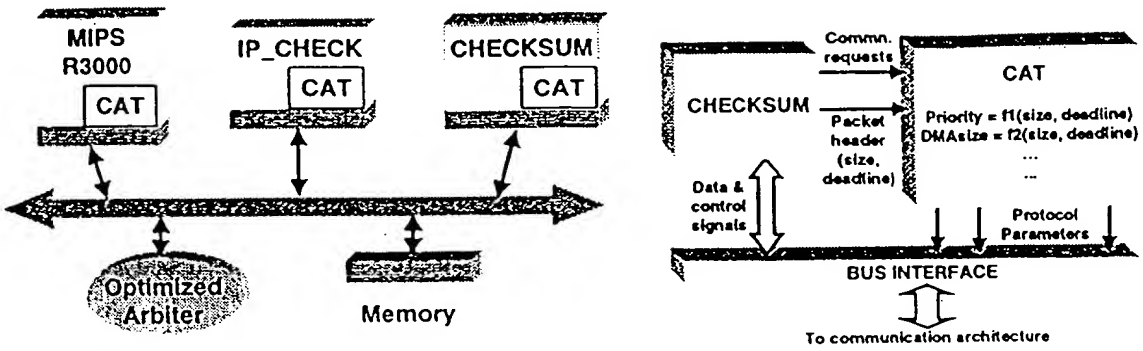

Pkt. i arrives
Pkt. i+1 arrives
Pkt. i+1 deadline
Pkt. i deadline
Pkt. j arrives
Pkt. j+1 arrives
Pkt. j deadline
Pkt. j+1 deadline
Case1:
checksum >
ip_check >
ether_driver
i
i+1
j
j+1
i+1 misses deadline
Case2:
ether_driver >
ip_check >
checksum
i
i+1
i
j
j+1
j
j+1
j misses deadline
ether_driver
ip_check
checksum

FIG. 2


MIPS
R3000
CAT
IP_CHECK
CAT
CHECKSUM
CAT
Optimized
Arbiter
Memory
Comm.
requests
CHECKSUM
Packet
header
(size,
deadline)
CAT
Priority = f1(size, deadline)
DMAsize = f2(size, deadline)
...
Data &
control
signals
Protocol
Parameters
BUS INTERFACE
To communication architecture

(a) (b)

FIG. 3

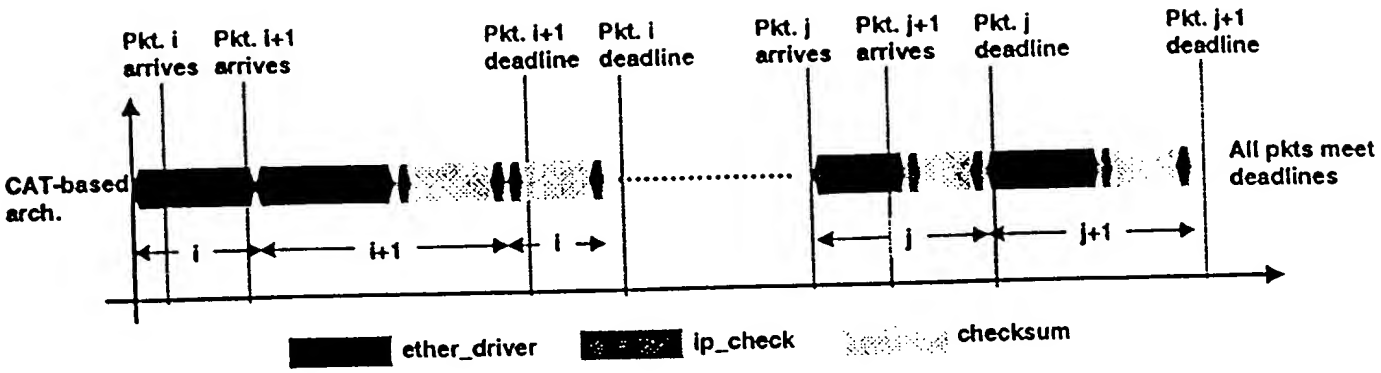

Pkt. i arrives
Pkt. i+1 arrives
Pkt. i+1 deadline
Pkt. i deadline
Pkt. j arrives
Pkt. j+1 arrives
Pkt. j deadline
Pkt. j+1 deadline
CAT-based arch.
All pkts meet deadlines
i
i+1
i
j
j+1
ether_driver
ip_check
checksum

FIG. 4

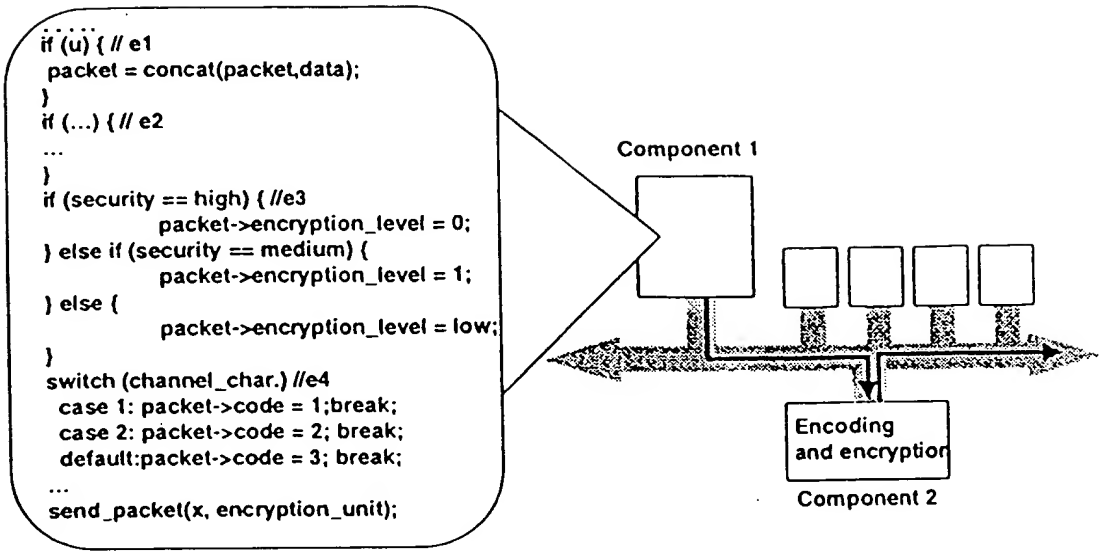

.....
if (u) { // e1
packet = concat(packet,data);
}
if (...) { // e2
...
}
if (security == high) { //e3
packet->encryption_level = 0;
} else if (security == medium) {
packet->encryption_level = 1;
} else {
packet->encryption_level = low;
}
switch (channel_char.) //e4
case 1: packet->code = 1;break;
case 2: packet->code = 2; break;
default:packet->code = 3; break;
...
send_packet(x, encryption_unit);
Component 1
Encoding
and encryption
Component 2

FIG. 5

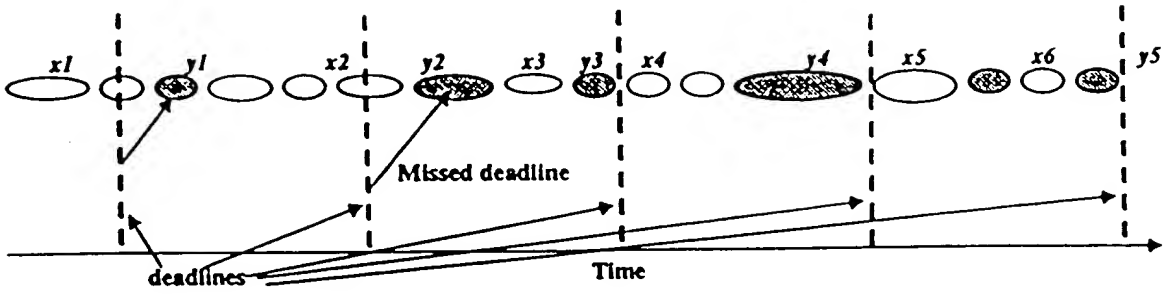


FIG. 6

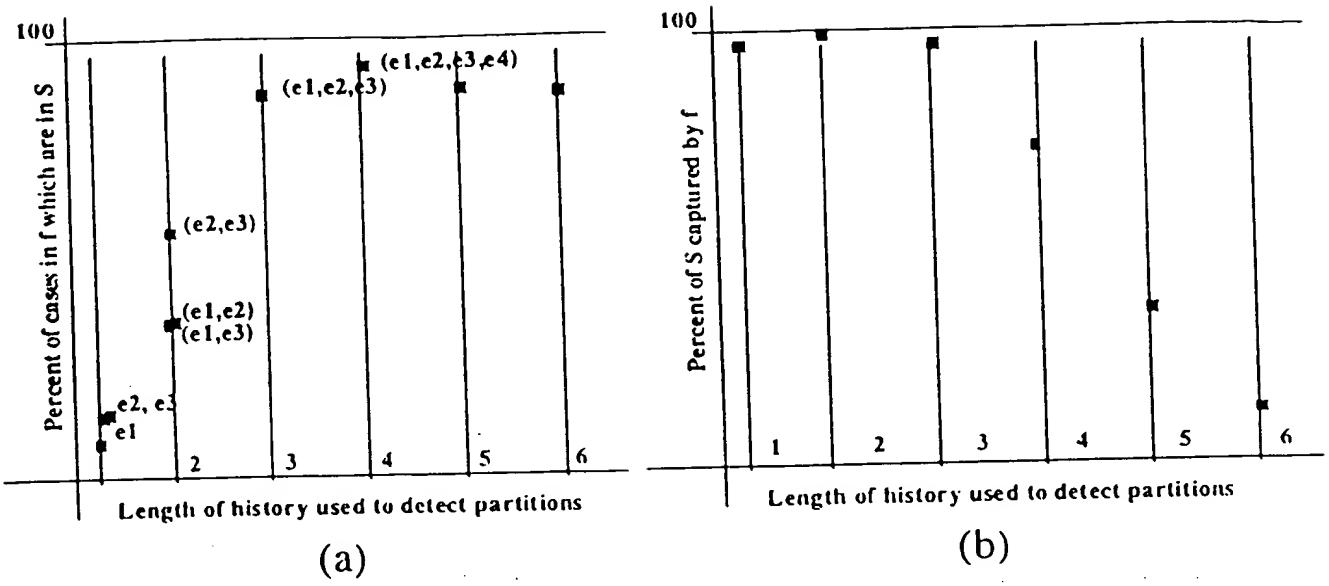

100
Percent of cases in f which are in S
(e1,e2,e3,e4)
(e1,e2,e3)
(e2,e3)
(e1,e2)
(e1,e3)
e2, e3
e1
2
3
4
5
6
Length of history used to detect partitions
(a)
100
Percent of S captured by f
1
2
3
4
5
6
Length of history used to detect partitions
(b)

FIG. 7

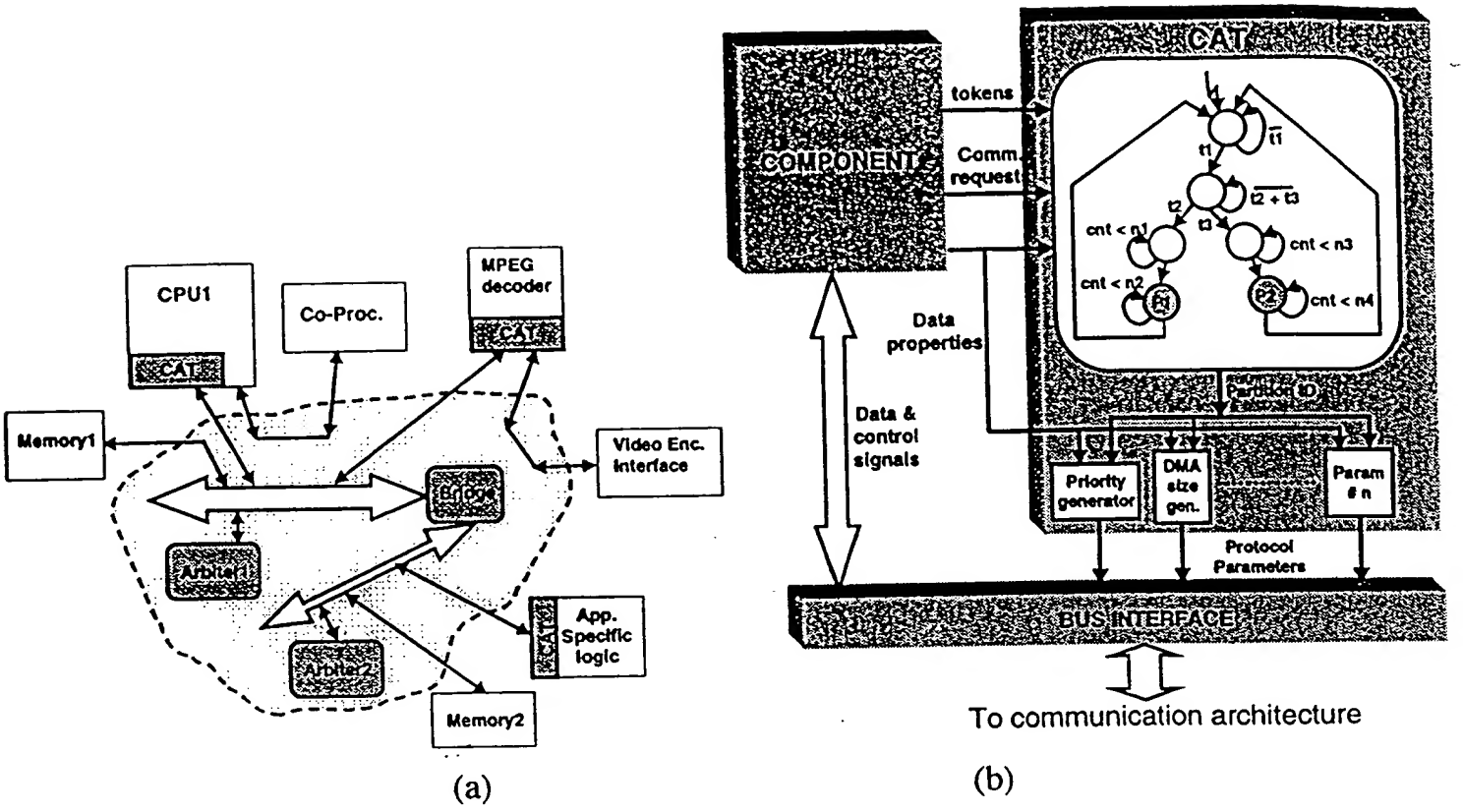

CPU1
CAT
Co-Proc.
MPEG decoder
CAT
Memory1
Video Enc. interface
Bridge
Arbiter1
Arbiter2
App. Specific logic
CAT
Memory2
(a)
CAT
COMPONENT
tokens
Comm. request
Data properties
Data & control signals
t1
t2
t3
cnt < n1
cnt < n2
cnt < n3
cnt < n4
P1
P2
Priority generator
DMA size gen.
Param # n
Protocol Parameters
BUS INTERFACE
To communication architecture
(b)

FIG. 8

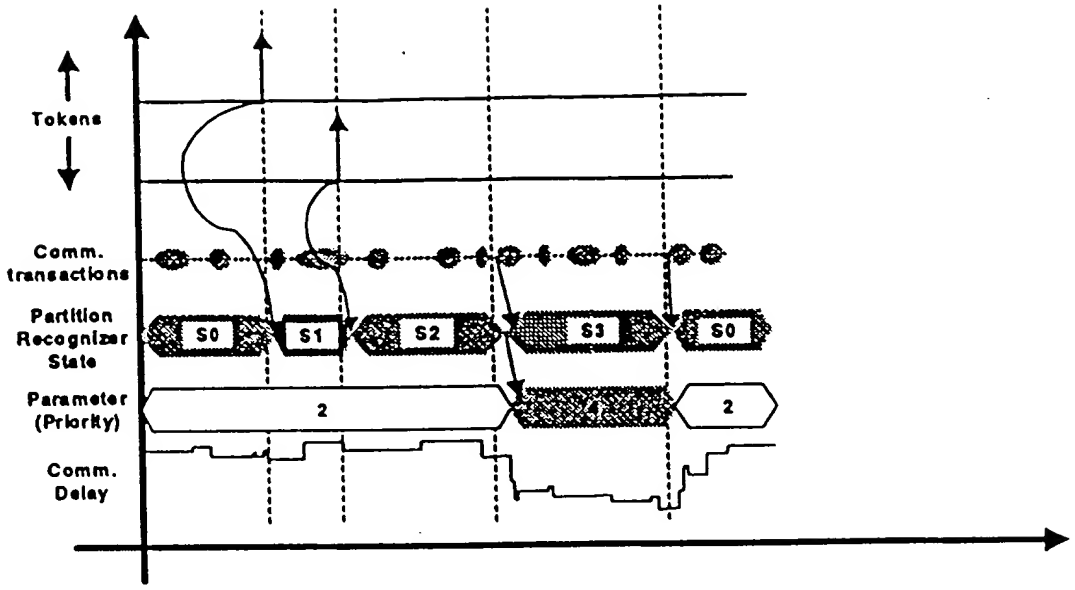

Tokens
Comm. transactions
Partition Recognizer State
S0
S1
S2
S3
S0
Parameter (Priority)
2
2
Comm. Delay

FIG. 9

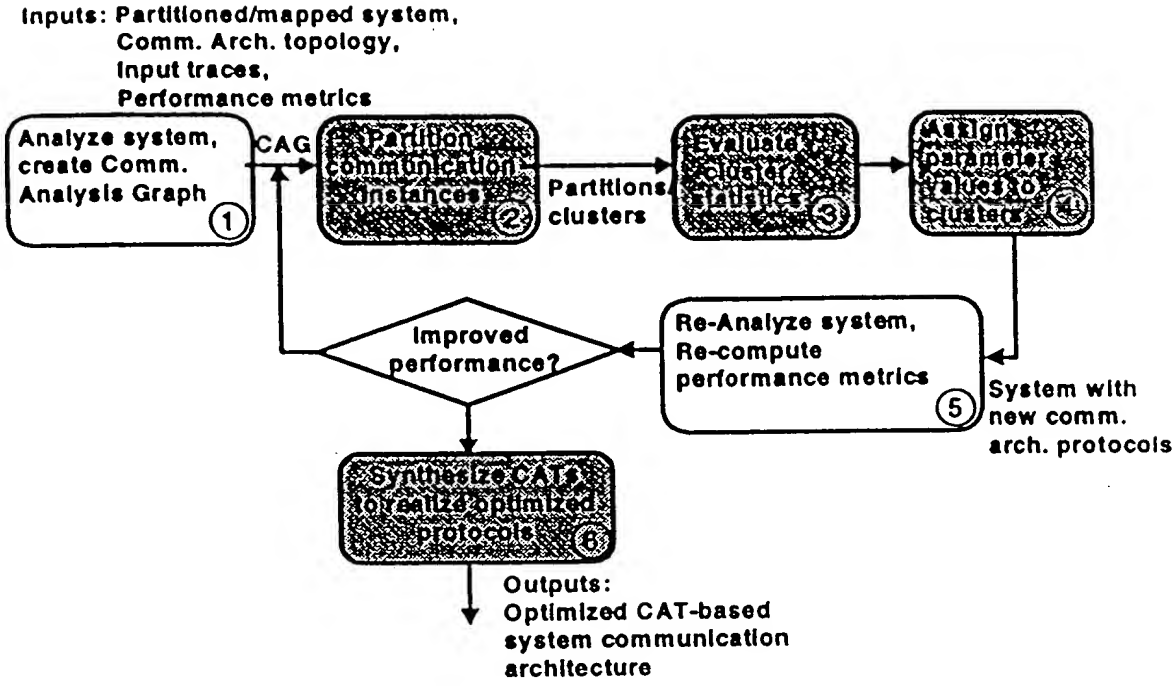

Inputs: Partitioned/mapped system,
Comm. Arch. topology,
Input traces,
Performance metrics
Analyze system, create Comm. Analysis Graph
1
CAG
Partition communication instances
2
Partitions/ clusters
Evaluate cluster statistics
3
Assign parameters values to clusters
4
Re-Analyze system, Re-compute performance metrics
5
System with new comm. arch. protocols
Improved performance?
Synthesize CATs to realize optimized protocols
6
Outputs:
Optimized CAT-based system communication architecture

FIG. 10

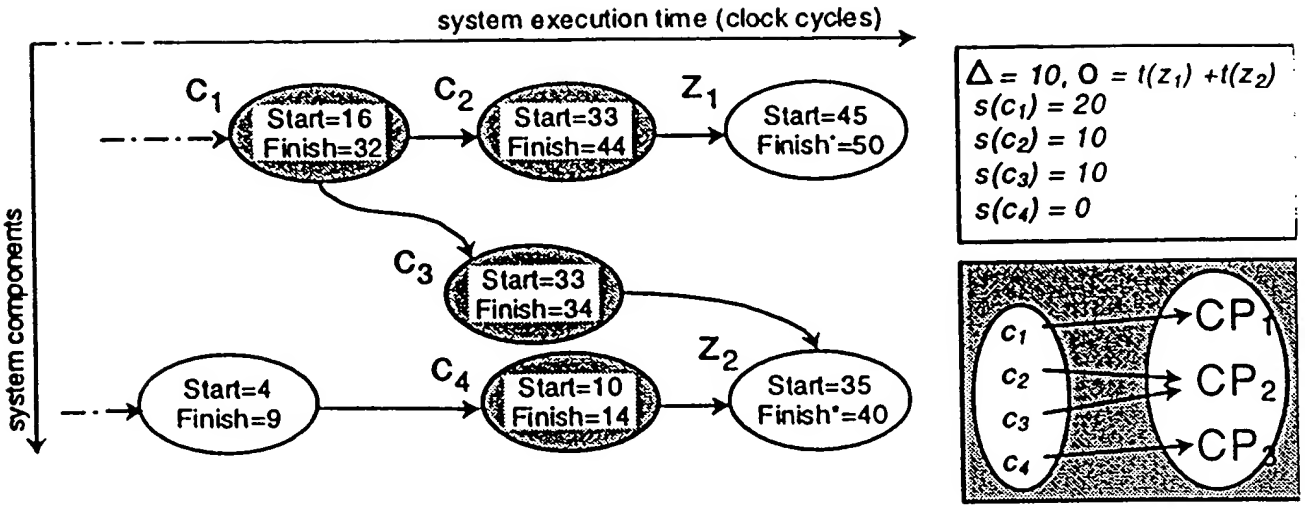

system execution time (clock cycles)
system components
C1
Start=16
Finish=32
C2
Start=33
Finish=44
Z1
Start=45
Finish*=50
C3
Start=33
Finish=34
Z2
Start=4
Finish=9
C4
Start=10
Finish=14
Start=35
Finish*=40
Δ = 10, O = t(z1) +t(z2)
s(c1) = 20
s(c2) = 10
s(c3) = 10
s(c4) = 0
c1
c2
c3
c4
CP1
CP2
CP3

FIG. 11

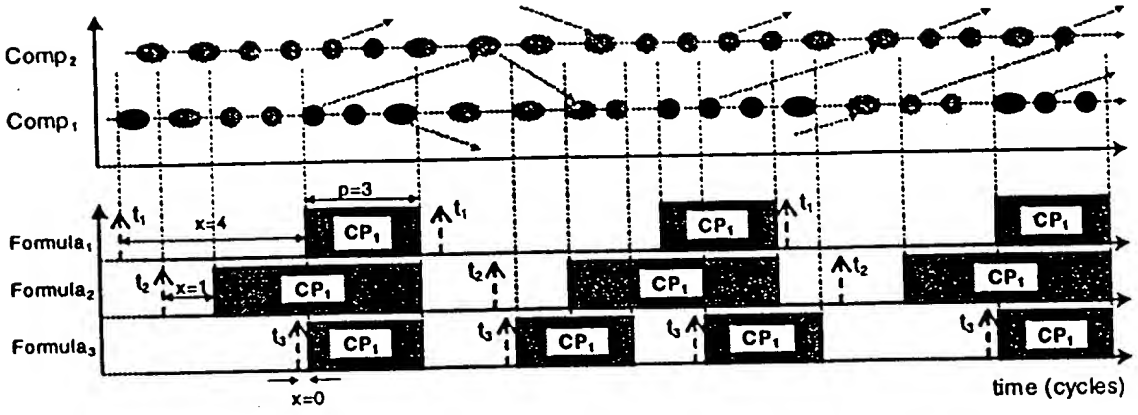

Comp2
Comp1
p=3
t1
x=4
CP1
Formula1
t2
x=1
Formula2
t3
Formula3
x=0
time (cycles)

FIG. 12

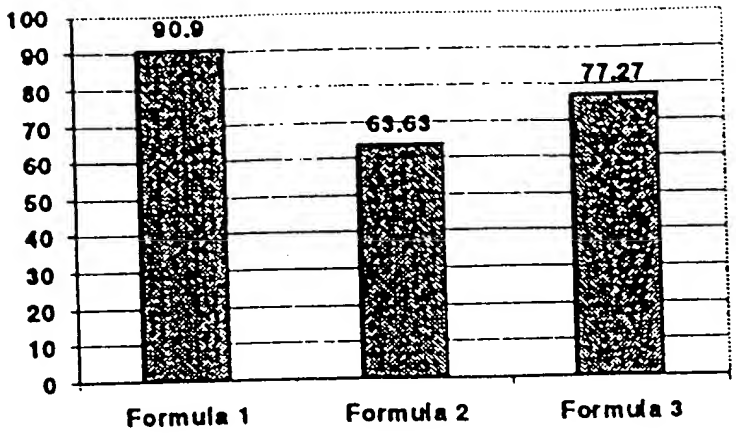

100
90
80
70
60
50
40
30
20
10
0
90.9
63.63
77.27
Formula 1
Formula 2
Formula 3

FIG. 13

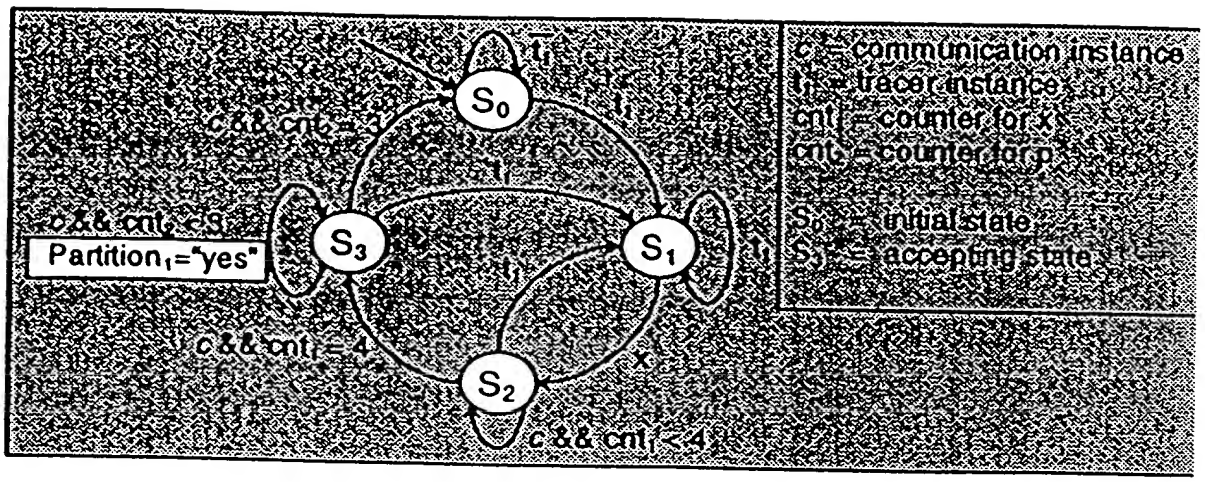

S_0
S_1
S_2
S_3
Partition$_1$="yes"
c && cnt$_c$ = 3
c && cnt$_c$ < 3
c && cnt$_t$ = 4
c && cnt$_t$ < 4
c = communication instance
t$_i$ = trace instance x, y
cnt$_t$ = counter for x's
cnt$_c$ = counter for p's
S_0 = initial state
S_3 = accepting state

FIG. 14

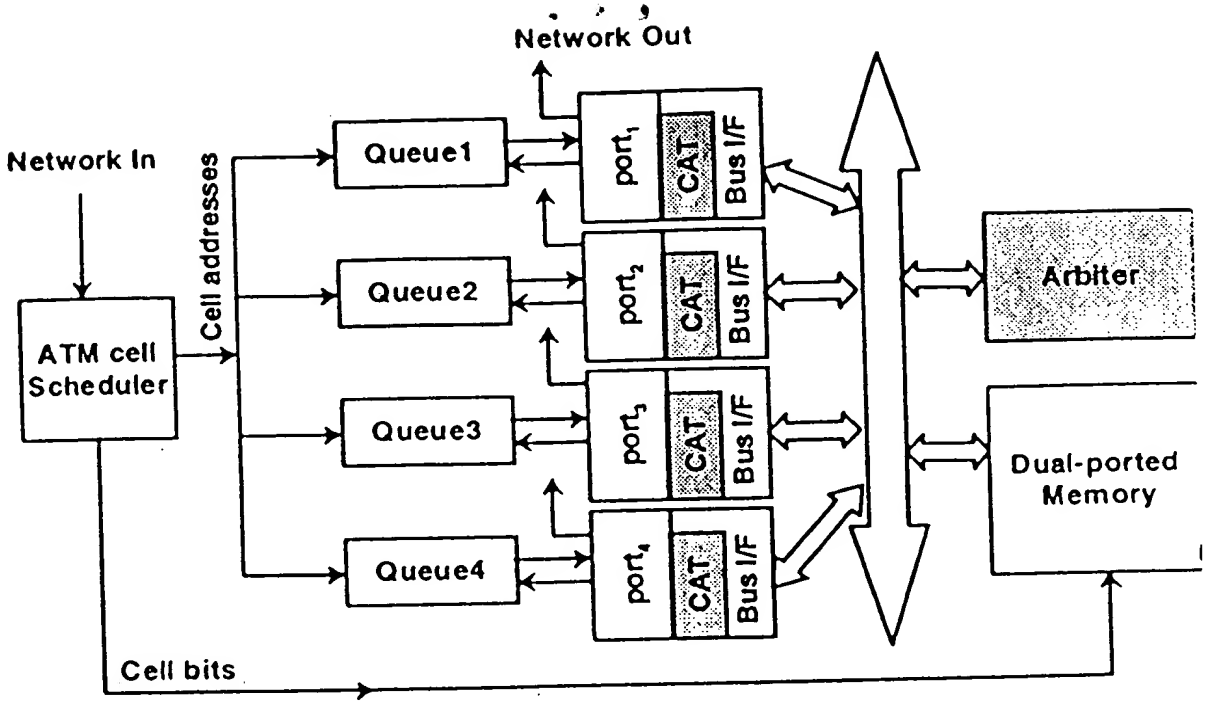

Network Out
Network In
Cell addresses
Queue1
Queue2
Queue3
Queue4
ATM cell Scheduler
port1
port2
port3
port4
CAT
Bus I/F
Arbiter
Dual-ported Memory
Cell bits

FIG. 15

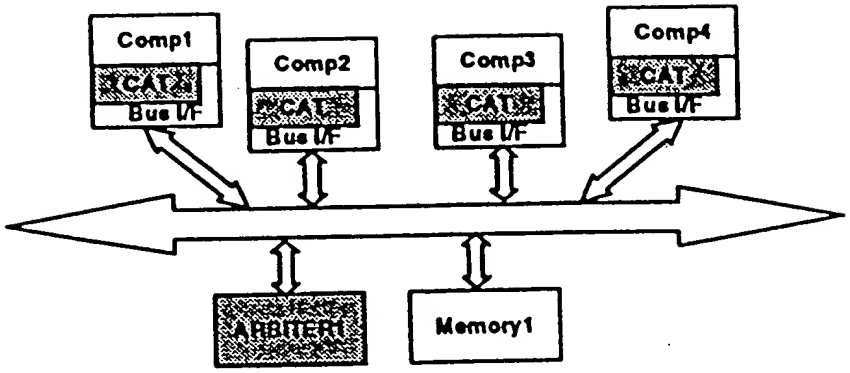

Comp1
CAT
Bus I/F
Comp2
CAT
Bus I/F
Comp3
CAT
Bus I/F
Comp4
CAT
Bus I/F
ARBITER
Memory1

FIG. 16

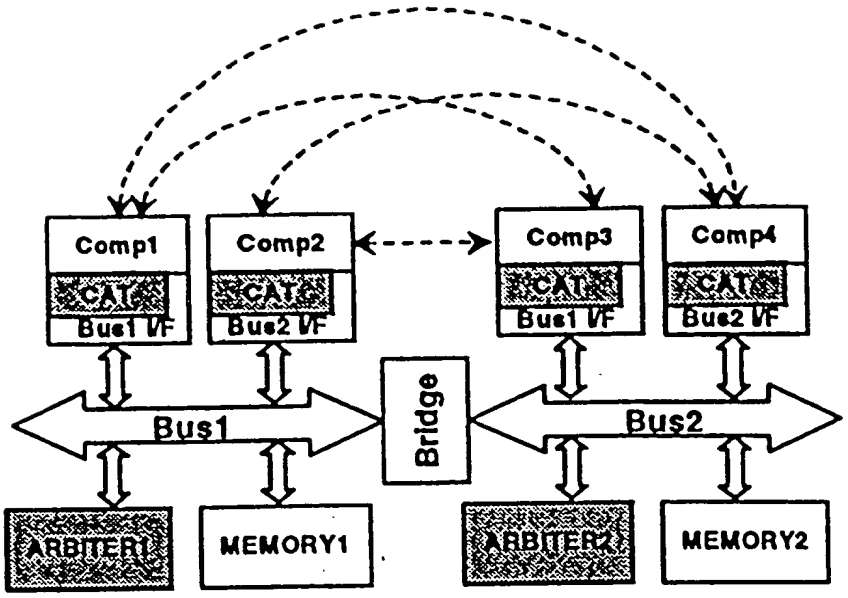

Comp1
CAT
Bus1 VF
Comp2
CAT
Bus2 VF
Comp3
CAT
Bus1 VF
Comp4
CAT
Bus2 VF
Bus1
Bridge
Bus2
ARBITER1
MEMORY1
ARBITER2
MEMORY2

FIG. 17